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CONFIGURABLE DECODER FOR ADDRESSING A MEMORY

ABSTRACT OF THE DISCLOSURE

Methods and apparatus for decoding addresses in a memory to provide mixed input and output data widths. A method includes receiving an address portion comprising a first number of bits. A second number of bits of the address portion are blocked, where the second number is less than the first number. A third number of bits are not blocked, and the third number plus the second number equal the first number. The third number of bits are decoded and a fourth number of memory cells are selected. The fourth number is equal to two to the power of the second number. A fourth number of data bits are received and multiplexed to the selected memory cells. The data bits are written to the selected memory cells.

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